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09/747,052	12/22/2000	Eugene D. Ham III	4015-808	1573

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EXAMINER	
WANG, TED M	

ART UNIT	PAPER NUMBER
2634	5

DATE MAILED: 08/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/747,052	HAM, EUGENE D.	
	Examiner	Art Unit	
	Ted M Wang	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 June 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,8-12,24-28,32-35 and 37-39* is/are rejected.

7)☒ Claim(s) *6,7,13-23,29-31 and 36* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 June 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-39 are pending in the application.

Response to Arguments

2. Applicant's arguments, paper # 4, filed on June 7, 2004, have been fully considered but they are not persuasive. The Examiner has thoroughly reviewed Applicants' arguments but firmly believes that the cited reference to reasonably and properly meet the claimed limitations.

Independent Claims 1, 10, and 24

(1) *Applicants' argument* – "Claim 1 requires, "adapting a filter based on average control values determined from said successive control values." That is, the control logic of the present invention bases adjustments to the loop filter on the values of the loop filter output. The patent to Wilhelmsson, however, fails to teach this element. .. Notably, however, adjustments to the filter circuit parameters in Wilhelmsson are not "based on average control values determined from ... successive control values," as required by claim 1."

Examiner's response -- In response to applicant's argument that the cited patent Wilhelmsson (US6,353,647) does not teach or suggest those limitations of claim 1 "adapting a filter based on average control values determined from said successive control values.", the Wilhelmsson Patent discloses a phase locked loop having phase detector, a filter circuit, a DAC, a VCO, and a filter circuit controller to control the filter circuit as described column 11 line 49 – column 12

line 28 and Fig.12 elements 2, 3, 9, 13, and 44. Referring to Fig.12, the filter circuit 44 is a digital low pass filter and inherently it outputs an averaged control signal. The filter control 13 receives the output signal of the digital filter circuit 44 and checks whether or not the voltage corresponding to the output signal from the digital filter circuit 44 lies within a predetermined portion of the control voltage range of the DAC 3 and/or the VCO 9. Clearly, the filter 44 is controlled by the controller 13 that is based on average control signal feedback from filter 44 output. Regarding claims 10 and 24, they too contain language similar to that of claim 1. Specifically, claim 10 requires, "adapting a filter characteristic of said digital filter based on said average control values," and claim 24 requires, "control logic to control a filter characteristic of said loop filter based on an average control value determined from successive ones of said control values to minimize clock deviations in output signal." Thus, for the explanation addressed in the above paragraph, the rejection under 35 U.S.C. 102(e) with Wilhelmsson's reference is adequate.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 1-5, 8-11, 24-28, 32, 34, 35, and 37-39 are rejected under 35 U.S.C. 102(e) as being anticipated by Wilhelmsson et al. (PT6,353,647).

- In regard claim 1, Wilhelmsson et al. discloses a phase locked loop having the method comprising determining successive phase difference values between a reference clock signal and said output clock signal (Fig.4-6, 10, 12, and 14 element 2D, and column 5 line 54 – column 6 line 50); filtering said successive phase difference values to generate successive control values (Fig.4-5 element 4D, Fig.6 and 14 element 4D', Fig.10 and 12 element 44, and column 5 line 54 – column 6 line 50); controlling a frequency of said output clock signal based on said successive control values (Fig.4-6, 10, 12, and 14 element 3, and column 6 lines 13-16); and adapting said filter based on average control values determined from said successive control values (Fig.12 and 14 elements 13a-13c, and column 11 line 49 – column 12 line 27 and column 13 line 5 – column 14 line 12).
- In regard claim 2, the limitation of detecting a trend in said average control values and determining a filter state based on said trend in said average control values can further be taught in Fig. 12-14, and column 11 line 49 – column 12 line 41.
- In regard claim 3, the limitation of selecting a fast filter setting for said filter when said trend indicates that said average control values have not stabilized can

further be taught in column 13 line 7 – column 14 line 28, and column 2 line 53 – column 3 line 18.

- In regard claim 4, the limitation of a slow filter setting for said filter when said trend indicates that said average control values have stabilized can further be taught in column 13 line 7 – column 14 line 28 and column 2 line 53 – column 3 line 18.
- In regard claim 5, the limitation of determining difference values between successive ones of said average control values, and wherein adapting said filter based on said average control values determined from said successive control values comprises adapting said filter based on processing said difference values can further be taught in column 9 lines 51 – column 10 line 60 and column 12 lines 7-23.
- In regard claim 8, the limitation of adapting said filter based on processing said difference values comprises: identifying peak values in said difference values; and adapting said filter based on said peak values (or gains) can further be taught in column 9 line 51 – column 10 line 60, and column 13 line 7 – column 14 line 28.
- In regard claim 9, the limitation of adapting said filter based on said peak values comprises setting said filter to a slow filter state if a summation of a number of successive peak values is below a defined threshold can further be taught in column 11 line 49 – column 12 line 41.

- In regard claim 10, which is a method of controlling a phase-locked loop (PLL) claim related to claim 1, all limitation is contained in claim 1. The explanation of all the limitation is already addressed in the above paragraph.
- In regard claim 11, which is a method of controlling a phase-locked loop (PLL) claim related to claim 3 and 4, all limitation is contained in claim 3 and 4. The explanation of all the limitation is already addressed in the above paragraph.
- In regard claim 24, Wilhelmsson et al. discloses a controllable oscillator providing an output signal at a frequency proportionate to an oscillator control signal (Fig.4-6, 10, 12, and 14); a phase detector providing a phase error signal by detecting a phase difference between an input signal and said output signal (Fig.4-6, 10, 12, and 14 element 2D, and column 5 line 54 – column 6 line 50); an adjustable loop filter providing control values based on filtering said phase error signal (Fig.10 and 12 element 44, and Fig.14 element 4D'); a control circuit providing the oscillator control signal responsive to said control values (Fig.10, 12, and 14 element 3); and control logic to control a filter characteristic of said loop filter based on an average control value determined from successive ones of said control values to minimize clock deviations in said output signal (Fig.10, 12, and 14 element 13). The explanation of all the limitation is already addressed in the above paragraph.
- In regard claim 25, the limitation that control logic is operable in one of a defined number of states, and further wherein said control logic adjusts said filter characteristic of said loop filter based on a current state of said control logic can

further be taught in column 13 line 7 – column 14 line 28, and column 2 line 53 – column 3 line 18.

- In regard claim 26, the limitation that control logic transitions from a first state to a second state based on at least one characteristic of said average control values can further be taught in column 13 line 7 – column 14 line 28, and column 2 line 53 – column 3 line 18.
- In regard claim 27, the limitation that control logic transitions from a first state to a second state based on at least one characteristic of said average control values can further be taught in column 13 line 7 – column 14 line 28, and column 2 line 53 – column 3 line 18.
- In regard claim 28, the limitation that control logic adjusts said filter characteristic of said loop filter based on a difference between successive average control values can further be taught in column 9 lines 51 – column 10 line 60 and column 12 lines 7-23.
- In regard claim 32, the limitation that loop filter comprises a digital loop filter adapted to output said control value in a digital format (Fig.10 and 12 elements 44 and 3, and Fig.14 elements 4D' and 3).
- In regard claim 34, the limitation that control circuit is a digital-to-analog converter (DAC), and further wherein said control value provided by said loop filter is a digital value conforming to an input range of said DAC such that said DAC generates a control voltage as said oscillator control signal relative to said digital value can further be taught in Fig.10 and 12 elements 44 and 3, and Fig.14

elements 4D' and 3, and column 11 line 49 – column 12 line 41 and column 13 line 7 – column 14 line 12.

- In regard claim 35, the limitation that controllable oscillator is a voltage-controlled oscillator (VCO), and further wherein said VCO generates said output signal at a frequency determined by a value of said control voltage generated by said DAC can further be taught in Fig. 12 and 14 element 9 and 3, and column 11 lines 54-57, column 12 lines 7-20 and column 13 line 66 – column 14 line 1.
- In regard claim 37, the limitation that control operates in one of a defined number of states, with each of said states corresponding to a desired filter setting for said loop filter, and to control transitions between said states based on processing average control values determined from said control values can further be taught in column 9 line 51 – column 10 line 60 and column 11 line 49 – column 12 line 28.
- In regard claim 38, all limitation is contained in claim 37. The explanation of all the limitation is already addressed in the above paragraph.
- In regard claim 39, the limitation that control logic comprises a digital processor can further be taught in Fig. 10, 12, and 14, and column 9 lines 59-66.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject

matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 12 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wilhelmsson et al. (PT6,353,647) in view of Glass (PT5,619,543).

- In regard claim 12, Wilhemsson et al discloses all of the limitation as described in the above paragraph except specifically teaching that digital filter is a proportional-integral (P-I) digital filter.

  Glass discloses a digital phase-locked loop filter with a proportional-integral type digital PLL filter (Fig.3 and 4, and column 2 line 60 – column 4 line 23) in order to use a relatively high coefficient K_L to ensure fast control during the initial phase, and once the communication is established to decrease coefficient K_L (and more generally the filtering coefficients K) to carry out small corrections and to ignore high instantaneous variations normally corresponding to non-repetitive parasitic pulses.

  It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Wilhemsson's PLL in view of Glass's disclosure in order to use a relatively high coefficient K_L to ensure fast control during the initial phase, and once the communication is established to decrease coefficient K_L (and more generally the filtering coefficients K) to carry out small corrections and to ignore high instantaneous variations normally corresponding to non-repetitive parasitic pulses.

- In regard claim 33, which is a PLL claim related to claim 12, all limitation is contained in claim 12. The explanation of all the limitation is already addressed in the above paragraph.

Allowable Subject Matter

5. Claims 6, 7, 13-23, 29-31, and 36 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

1. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ted M Wang whose telephone number is (703) 305-0373. The examiner can normally be reached on 8:30 a.m. - 5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven Chin can be reached on (703) 305-4714. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 306-0377.

Ted M Wang
Examiner
Art Unit 2634

Ted M. Wang

SHUWANG LIU
PRIMARY EXAMINER